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Novel capacitor clamped balanced 9 level reduced switch topology for drive applications

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Abstract

The development of switched-capacitor multilevel inverters (SCMLIs) is a response to the growing need for power quality and capacity improvements. Modern SCMLIs allow for step-up ac output via inversion and single-stage voltage boosting. This study presents a boost type singlesource nine-level (9-level) SCMLI that uses two capacitors and three diodes in an effort to reduce the number of components. You may quadruple the voltage increase from a single source by using capacitors, which have balanced voltages due to the series-parallel connection procedure. There is a strict restriction of twice the input voltage for maximum voltage stress across semiconductor devices. You can enhance the proposed SCMLI to boost voltage levels without extra dc input using a minimum number of components. The maximum voltage stress remains the same as in the 9-level circuit, but each extension module increases the output voltage by two steps. A comprehensive comparison of newly-developed single-phase 9-level MLIs is then performed, confirming design superiority, after which a detailed analysis of circuit functioning and power losses is performed. The key characteristics of the 9-level SCMLI are validated under dynamic operating settings through extensive experimental and simulation results.

Key Words: switched-capacitor multilevel inverters, 9-level inverter and Voltage stresses

I. Introduction

A variety of power converters have been studied for effective power conversion in response to the growing demand for clean power generation. One type of converter that is essential for making high-quality ac output from dc input is the multilevel

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inverter (MLI). A sinusoidal-like output can be synthesised by MLIs using a combination of dc sources, switches, diodes, and capacitors. Because of its little distortion, an MLI's output can enhance power quality while reducing filter size [1, 2]. The usage of MLIs, as opposed to three-level inverters, is more common in medium-high power conversion systems, including electric drives, wireless power transmission, photovoltaic (PV) systems, and many more [3]-[6]. Flying capacitor (FC), neutral-point clamped (NPC), and cascaded Hbridge (CHB) MLI are the most common types of MLIs [3], [7]-[9]. An increase in voltage causes the circuit to become more complex since FC MLI requires an additional capacitor and NPC MLI requires additional diodes. Concerning these topologies in particular, voltage imbalance and module failure are major difficulties [10], [11]. As an alternative, CHB MLI is simpler, has versatility, and can withstand faults. While CHB MLIs with multiple sources can operate in either asymmetrical or symmetrical modes, depending on the magnitude of the dc sources, the increased number of switches and the demand for numerous sources remain issues.

The aforementioned problems inspired the development of reduced switch MLIs in [12]-[14]. For use in standalone applications, the symmetrical construction described in [12] combines PV panels with battery storage units. In order to allow load current backflow under inductive loading conditions, the symmetrical MLI in [13] can be coupled with an extra switch using the architecture described in [15]. By incorporating a self-balanced level doubling module, an asymmetrical architecture for PV application—as suggested in [14]—dramastically decreases the amount of components per level. The usage of an H-bridge, which raises total voltage stress (TVS), the need for the management of several PV panels, and the inability to boost voltage are all problems that will inevitably arise with these structures, even though they are being developed as a new way to reduce the number of switches.

MLIs find extensive use in photovoltaic (PV) systems that must boost voltage in order to meet grid or load standards; this is the case when the input voltage is low and must be increased. On the flip side, MLI topologies without inductors and transformers are required for compact converter sizing. This can be accomplished with the aid of input sources and a combination of switched-capacitors (SCs), according to the literature. The input voltage can be increased by charging SCs in

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parallel with it and then discharging them in series. One switching period is used to alternately charge and discharge the capacitors, as suggested in [16], [17] for voltage balancing control. Therefore, it is possible to reduce the number of sources while keeping the ripple voltage on the capacitors low. Traditional CHB MLIs are formed from a single dc source in an effort to decrease the number of input sources [5], [18]. There is no need for supplementary inductors or transformers in these configurations to generate 5-level or 9-level output. To keep the necessary voltage between the capacitors, however, an auxiliary voltage balancing control is necessary. Furthermore, in order to decrease total size and expense, it is recommended to avoid these topologies due to the high number of switches they require. Additionally, higher voltage level synthesis can be accomplished using the 9-level circuits that were established in [7], [19], and [20]. Nevertheless, the voltage gain in these topologies is constrained to one, and the TVS is increased by a polarity reversal H-bridge in [7], [19].

In an effort to create structures that utilise the inherent voltage boosting SC method, which is beneficial for PV applications, generalised MLIs have been suggested in [21], [22]. A basic module with one source, one capacitor, one diode, and two switches is the basis of the generalised MLI described in [21]. The capacitor, which aids in inherent voltage boosting, can be charged and discharged with the use of these switches. Extending this architecture in both symmetrical and asymmetrical directions necessitates a substantial amount of switches. Using series diodes, the single-dc MLI described in [22] is unable to function when subjected to low power factor (PF) loads. Two diodes and two capacitors make up the front-end circuit of a nine-level single-input MLI that is described in reference [23]. The circuit's capacitors are charged to half the magnitude of the input voltage, limiting voltage boosting to twice the input. In addition, these topologies have an H-bridge at the backend, which increases the TVS. This is how new generalised MLIs were suggested in [24] and [25], avoiding the need for a full bridge at the back end. If you want larger voltage levels at the output, though, you'll need a combination of symmetrical and asymmetrical sources. Reducing the amount of capacitors is the goal of the generalised circuit topology described in [26]. But it can't get around the need

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for more than one source. A single dc source and a minimum number of capacitors are used to construct 9-level MLIs in [27]-[29] to address this issue. In this case, the voltage gain can't be more than double the magnitude of the input voltage. High step-up single-input SCMLIs have also been reported in recent literature. In addition to drastically lowering voltage stress, the structure in [33] can be easily expanded to generate larger voltage levels, however doing so requires an excessive amount of switches. The generalised circuit drastically cuts down on the amount of switches [34]. Some switches, though, are rated at maximum output voltage. Both [31] and [30] propose 9-level quadruple boost MLIs with the same number of switches; however, [31] uses three capacitors and [30] uses two. The circuit shown in reference [35] drastically cuts down on the number of switches. The three capacitors used are comparable to the MLI in [31], and two of the switches have a peak output voltage rating. Four switches with a peak output voltage rating are necessary for a newly suggested 9-level MLI [32]. Considering the drawbacks of the current 9-level structures shown in Figure 1, this study suggests a simplified switch SCMLI that has the following notable characteristics:

II. Design of Test system

a) Principle Of Operation Of Proposed 9-Level Scmli

A single dc source (Vin) and ten switches (S1- S10) make up the proposed single-phase 9-level SCMLI, as shown in Figure 1. Separating the circuit into two modules will make analysis much easier. Each module has a different combination of components; M1 uses two switches (S1, S2), one diode (D1), and one capacitor (C1), whereas M2 uses four switches (S3-S6), two diodes (D2, D3), and one capacitor (C2). The input voltage is doubled by the M1, and its output is further doubled by the M2.

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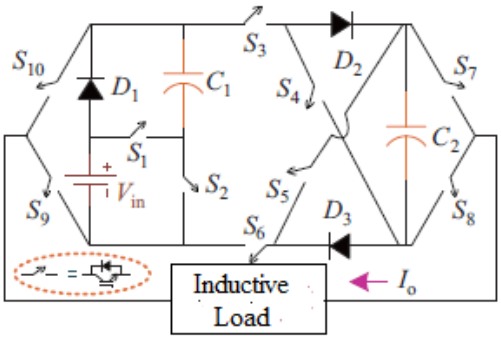

Figure 1 Proposed 9-level quadruple boost SCMLI topology.

4Vin) by keeping the voltage ratio between capacitors C1 and C2 at 1:2. A more straightforward functioning of the circuit is achieved by the complementary action of the switch pairs (S1, S2), (S3, S5), (S4, S6), (S7, S8), and (S9, S10). To further eliminate source short circuiting, it is not recommended to operate (S3, S4, S6) and (S3, S5, S6) switch combinations simultaneously. When switch S1 is turned off, only then is diode D1 forward biassed; nevertheless, when the switch-pair (S4, S5) is turned off, diodes D2 and D3 become forward biassed.N3Vin, N2Vin, NVin, NBypassing the end-side complete bridge, the switches (S7–S10) are configured to generate the necessary ac output. Consequently, M1 devices are subject to Vin stress, while all other devices are capable of withstanding 2Vin stress. The suggested MLI generates a 9-level output. The next section discusses the operational analysis of the proposed circuit, ignoring the voltage drop across semiconductor devices and assuming capacitors can maintain a steady-state voltage in the ratio Vin: 2Vin. Capacitor C1 is discharged and capacitor C2 is charged when Vo = 0, because S1 from M1 and S3&Vin, capacitor C1 is charged by the conduction of switch S2. Both the positive and negative half-cycles have extra switches that are switched on: (S3, S4, S8, S9) and (S5, S6, S7, S10), respectively. C2 is a static capacitor. At Vo = 2Vin, the zero-level inconduction state is comparable to the switches from M1 and M2. You can reverse the polarity from positive to negative in consecutive voltage steps with the help of switch pairs (S7, S9) and (S8, S10). During the voltage drop of 3Vin, switch S2 opens and charges capacitor C1. C2 is discharged in series with the source as a result of the positive and negative half-cycles alternating between switch

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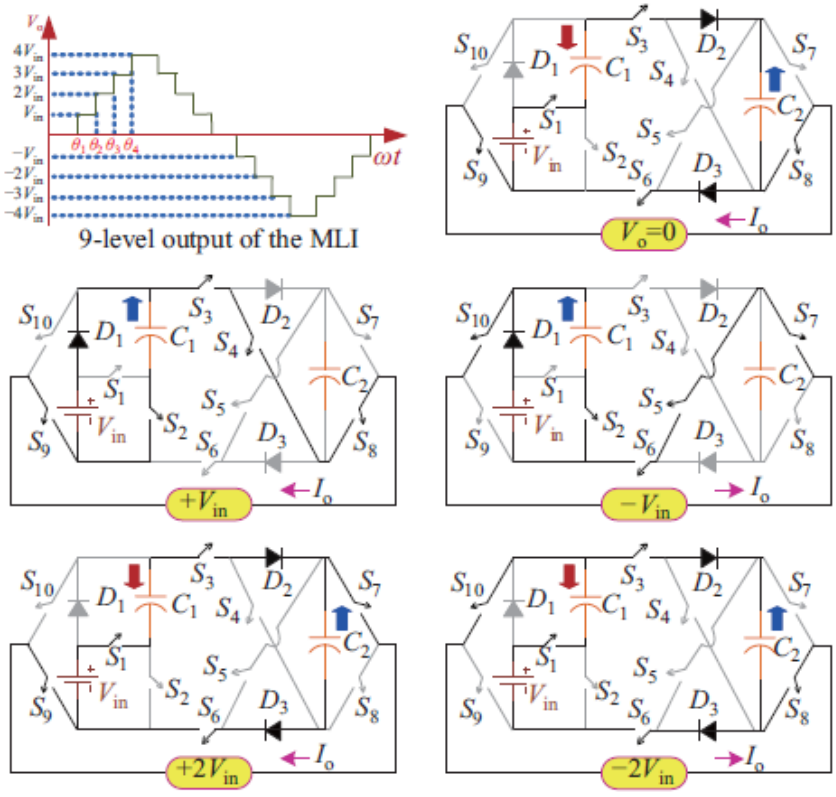
pairs (S3, S4) and (S5, S6) from M2. Comparable to the previous level, with the exception that switch S1 is now conducting, allowing for the discharge of both capacitors in series with the source, the peak output of 4Vin is achieved. Figure 3 displays the switching diagram with an inductive load in mind, which allows for successful operation with any type of load

b) Self-balancing Analysis and Capacitance Sizing

The charging and discharging processes of supercapacitors C1 and C2, respectively. According to Figures 3 and 5, C1 charges in parallel with the input supply during the intervals of Vin and 3Vin, while it discharges in series with the source at other times. Consequently, a steady-state voltage of Vin is sustained across C1. Conversely, C2 is charged at a zero level.



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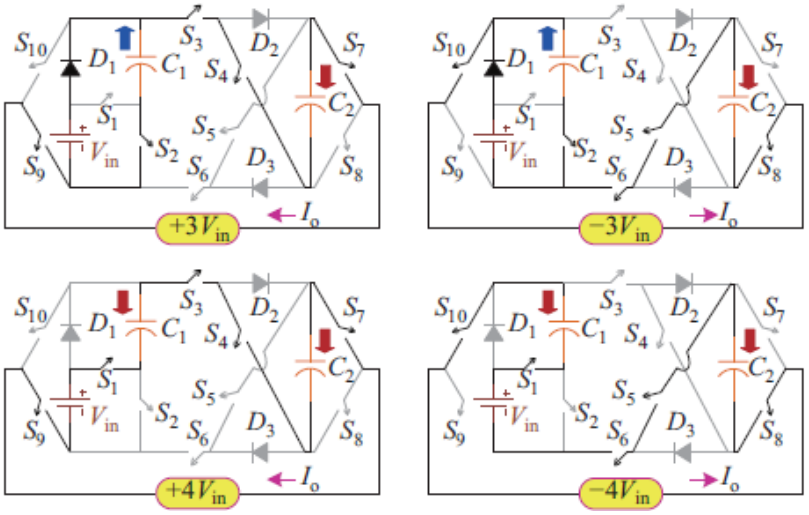

Figure 2 Operation of the proposed MLI considering inductive loading.

Table 4.1 Switching states

	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
4VDC	1	0	1	1	0	0	1	0	1	0
3VDC	0	1	1	1	0	0	1	0	1	0
2VDC	1	0	1	0	0	1	1	0	1	0
VDC	1	1	1	1	0	0	0	1	1	0
0	1	0	1	0	0	1	0	1	1	0
-VDC	1	0	1	0	0	1	0	1	0	1
-2VDC	1	0	1	0	0	1	0	1	0	1
-3VDC	0	1	0	0	1	1	0	1	0	1
-4VDC	1	0	0	0	1	1	0	1	0	1

simultaneously with M1 when M1's output is 2Vin. During 3Vin and 4Vin, it discharges in series with M1's output. The fundamental cycle's regular charging and discharging procedure keeps the voltage across C2 at a steady 2Vin. Additionally, (a) the time it takes to charge and discharge the capacitor is far shorter than the total output voltage duration, and (b) the low parasitic resistance channel guarantees that the capacitor voltages remain at the right level regardless of the loading.

The computation of an appropriate capacitance value is dependent on the nominal operating frequency (fn), load current (Io), voltage ripple (ΔVc) and

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maximum discharging period. From Fig. 3 it is clear that maximum discharging period of the SC C1 and C2 is from [θ4 to π − θ4] and [θ3 to π − θ3], respectively.

$$\Delta Q_{C1} = \frac{1}{\omega}\int_{\theta_4}^{\pi-\theta_4} I_{\text{omax}} \sin(\omega t - \varphi) \mathrm{d}\omega t$$

where φ is the phase angle and Iomax is the peak value of the load current. Taking into account a 10% maximum permitted voltage ripple, the value of capacitance is given by (3) and the maximum voltage ripple may be found in (2).

$$\Delta V_c = \frac{2I_{\text{omax}} \cos\theta_4 \cos\varphi}{\omega C_1}$$

$$C_1 = \frac{2I_{\text{omax}} \cos\theta_4 \cos\varphi}{0.1(\omega V_{\text{in}})}$$

Similarly, value of capacitance C2 is expressed as follows:

$$C_2 = \frac{I_{\text{omax}} \cos\theta_3 \cos\varphi}{0.1(\omega V_{\text{in}})}$$

c) Power Loss Evaluation For The Proposed SCMLI

You can think of the overall losses in SCMLIs as (a) losses during the switching transition, (b) losses during conduction caused by parasitic factors, and (c) losses during ripple generated by voltage ripple across the SCs. These losses are examined for the proposed MLI, taking into account resistive loading, at which the largest loss in any converter occurs.

d) Switching Loss Analysis

Any power converter will experience switching losses as a result of the rapid transition from the on to off state of the switching mechanism. The linear capacitance variation provides the basis for calculating these losses [23]. In a linear fashion, the built-in capacitor (Csw) is charged when the standing voltage across the switch rises from zero to maximum (Vsw) as the switch is switched off. As soon as the switch is activated, the current carrying capacity (Csw) drains and the voltage drops from Vsw to zero. It is possible to express energy losses caused by switching transitions as

$$E_{\text{sw}} = \frac{C_{\text{sw}}}{2} {V_{\text{sw}}}^2$$

Therefore, switching power loss can be expressed as.

$$P_{\text{sw}} = f_s E_{\text{sw}} = \frac{C_{\text{sw}}}{2} f_s {V_{\text{sw}}}^2$$

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A fundamental frequency of 2Vin is clearly shown by the operational analysis in Figure 3 for the two switches S9 and S10. Despite being subjected to a combined voltage of 14Vin, the remaining eight switches function at a somewhat higher frequency (fs). Consequently, the following is the final expression of the Psw of the proposed SCMLI:

$$P_{sw} = \frac{C_{sw}}{2} V_{sw}{}^2 [4f_n + 14f_s]$$

e) Conduction Loss Analysis

Parasitic characteristics of conducting devices in the discharge loop are the primary culprits responsible for conduction loss. Three parasitic parameters are the forward voltage drop of diodes (VDeq), the equivalent parasitic resistance (Req) of the switch (when using anti-parallel diodes), and the equivalent series resistance (ESR) of the capacitors. Keeping this in mind, the discharging current loop shown in Figure 6 is equivalent, with RL representing the load resistance.

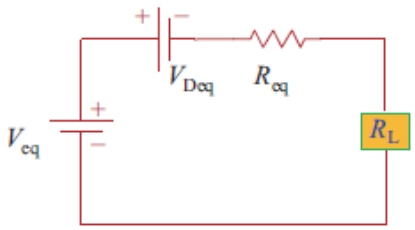

Figure 3 Equivalent current loop

Consider the following similar circuit parameters: RD internal resistance, RS on-state resistance, and VD forward voltage drop of all diodes (including anti-parallel diodes of switches):

Table 1 Equivalent Discharging Loop Parameters

Equivalent parameters	Equivalent voltage (V_{eq})	Forward voltage drop of diodes (V_{Deq})	Equivalent parasitic resistance (R_{eq})
$k = 0$	0	$2V_D$	$2(R_S + R_D)$
$k = 1$	V_{in}	$2V_D$	$3R_S + 2R_D$
$k = 2$	$2V_{in}$	V_D	$4R_S + R_D + ESR$
$k = 3$	$3V_{in}$	V_D	$4R_S + R_D + ESR$
$k = 4$	$4V_{in}$	0	$5R_S + 2ESR$

Considering a resistive loading condition, the overall conduction loss is expressed as,

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$$P_{\text{cn}} = \frac{2}{\pi}\sum_{k=1}^{4}\left\{\left(\frac{V_{\text{eq}} - V_{\text{Deq}}}{R_{\text{eq}} + R_{\text{L}}}\right)^2 \times R_{\text{eq}} \times (\theta_{k+1} - \theta_k)\right\}$$

4.3.3 Ripple Loss Analysis

Ripple loss, often called charging loss, is the power loss that occurs as a result of voltage ripples caused by continuously charging capacitors. The amount of energy lost during a single charging cycle as a result of a capacitor (C), regardless of parasitic resistance, can be determined as.

$$E_{\text{rip}} = \frac{1}{2}C\Delta V_c{}^2$$

If we assume a maximum permissible voltage ripple of 10% for the suggested SCMLI, we get the total ripple loss, which is

$$P_{\text{rip}} = f_n E_{\text{rip}} = f_n[C_1(0.1V_{\text{in}})^2 + C_2(0.2V_{\text{in}})^2]$$

Theoretical efficiency of the proposed SCMLI can be obtained by considering losses

$$\eta = \frac{\text{output power}}{\text{output power} + P_{\text{sw}} + P_{\text{cn}} + P_{\text{rip}}}$$

A comprehensive comparison is conducted with state-of-the-art 9-level (Nl) MLIs in order to evaluate the supremacy of the proposed 9-level SCMLI. Table II compares various components, including input sources (Ndc), driver circuits (Ndrv), diodes (Ndd), capacitors (Ncap), maximum number of switches in the conduction path (Nms), number of switches able to withstand peak voltage stress (Nsp), maximum voltage stress (MVS), total voltage drop (TVS), boosting ability (Cf), and cost factor (Cf). Whereas symmetrical topologies were suggested in [24], [26] and asymmetrical structures in [19], the most up-to-date architectures only need one input source. The suggested configuration uses a minimal number of components while achieving a high voltage gain with a minimum total voltage drop (TVS). To assign emphasis to the count of components and voltage stress, respectively, Cf incorporates a weightage coefficient β that is 0.5 and 1.5.

$$C_f = \frac{\begin{matrix}[N_{\text{sw}} + N_{\text{drv}} + N_{\text{dd}} + N_{\text{cap}} + N_{\text{ms}} + N_{\text{sp}} \\ +\beta(\text{TVS}_{\text{pu}} + \text{MVS}_{\text{pu}})]N_{\text{dc}}\end{matrix}}{N_l}$$

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The suggested SCMLI topology scores first among others in terms of the least cost factor under varied values of β, producing a 9-level high gain output while restricting MVS to 2Vin. When it comes to single-stage, single-phase power conversion systems, the suggested MLI is definitely the best option.

4.4 Recommended Extension Of The 9-Level SCMLI

The suggested MLI may be extended to generate Nl-level output, just like the generalised SCMLIs described in[21], [22], [24], [25], and [33]. With just one dc supply and n-numbers of extension modules (EM), the generalised circuit design depicted in Figure 7 can be described. Using four switches (Sna−Snd), one switching capacitor (Cna), and two diodes (Dna and Dnb), the suggested 9-level SCMLI is built, and the EM is just the M2 of this circuit.

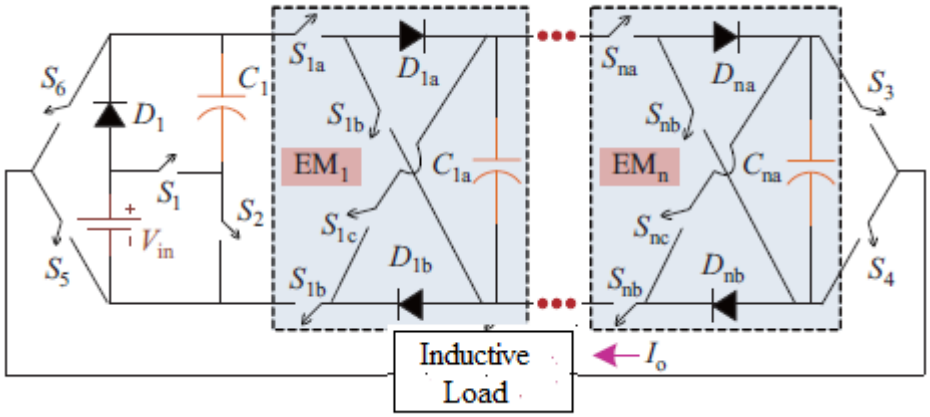

Figure 4 Proposed Nl-level circuit configuration

SCs in the expanded configuration exhibit intrinsic balance akin to the 9-level SCMLI. The charging and discharging of C1 and C1a–Cna resemble the operations depicted in Figures 4.5(a) and 4.5(b), respectively. The voltage across C1 is sustained at Vin, while capacitors C1a–Cna are symmetrically charged to 2Vin due to the concurrent conduction of switches S1a–Sna and S1d–Snd. Consequently, the generalised structure depicted in Fig. 4.7 generates voltage steps of 0, Vin, 2Vin, 3Vin, and (2n + 2)Vin utilising n EMs. Under symmetrical source voltages, the

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configurations presented in [24] and [25] have a voltage boosting capability that is double, regardless of the quantity of fundamental modules. Conversely, single input MLIs presented in [21], [22] have a voltage gain of (n + 1) times the input, utilising n fundamental modules. Conversely, the proposed generalised structure attains a substantial voltage amplification of (2n + 2) times the input. The quantity of levels, switch count, driver circuits, diodes, capacitors, and TVS in the expanded structure for n EMs can be articulated as follows:

$$N_l = 4n + 5$$
$$N_{\text{sw}} = N_{\text{drv}} = 4n + 6$$
$$N_{\text{dd}} = 2n + 1$$
$$N_{\text{cap}} = n + 1$$
$$\text{TVS}(\times V_{\text{in}}) = 8n + 10$$

Switches S1 and S2 are subject to a Vin voltage stress, but all other switches, regardless of voltage level, experience a 2Vin stress.

Vi. Simulation Verification

To validate operability of the proposed 9-level SCMLI, simulations are carried out using MATLAB/Simulink environment and the experimental results are obtained using a laboratoryscale prototype. Specifications of the test system are given in Table 2.

Table 2 Simulation Test Parameters

Parameters	Values
Input dc source (V_{in})	100 V
Capacitors (C_1 and C_2)	3300 μF (36 mΩ), 4700 μF (18 mΩ)
Nominal output frequency (f_{n})	50 Hz
Load 1 (R-load)	50 Ω
Load 2 (RL-load)	50 Ω-120 mH
Load 3 (RL-load)	60 Ω-150 mH

Switching pulses are obtained using fundamental frequency switching scheme [8], [9], [14] based on pre-computed angles. Using Fourier series, the 9-level staircase output waveform can be expressed mathematically as.

$$V_{\text{o}} = \sum_{n=1(\text{odd})}^{7} \frac{4V_{\text{in}}}{\pi}[\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4)]\sin(n\omega t)$$

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Peak fundamental voltage of the nth harmonic order can be further expressed as.

$$V_{n(\text{odd})} = \frac{4V_{\text{in}}}{\pi}[\cos(n\theta_1) + \cdots + \cos(n\theta_4)]$$

Therefore, harmonic equations can be derived neglecting higher order harmonics and without losing desired fundamental value as follows:

$$\begin{cases} n = 1 : 4M = \cos(\theta_1) + \cdots + \cos(\theta_4) \\ n = 3 : 0 = \cos(3\theta_1) + \cdots + \cos(3\theta_4) \\ n = 5 : 0 = \cos(5\theta_1) + \cdots + \cos(5\theta_4) \\ n = 7 : 0 = \cos(7\theta_1) + \cdots + \cos(7\theta_4) \end{cases}$$

For the proposed 9-level SCMLI, the modulation index (M) is given by

$$M = \frac{\pi V_1}{16V_{\text{in}}}, \quad 0 \leq M \leq 1$$

Considering the switching angle control as $0 < \theta1 < \theta2 < \theta3 < \theta4 \leq \pi/2$, the harmonic equations can be solved using the control technique in [14].

III. Simulation Analysis

To begin, we connect the proposed circuit to Load 1 and measure the output with different values of M. The load current pattern under pure resistive loading is the same as the 9-level load voltage waveform depicted in Figure 5.1(a). Even with a low M value of 0.15, the essential value remains unchanged. There is no auxiliary voltage balancing control used to keep the capacitor voltages at 100 V and 200 V, respectively. Figure 5.1 (b) shows the results of a harmonic analysis of the Vo.

Fig. 5 Simulation Results of the proposed 9-level SCMLI. (a) Output voltage, current and capacitor voltage under variation in modulation index. (b) Harmonic analysis of the output voltage at M = 0.15, 0.6 and 0.95

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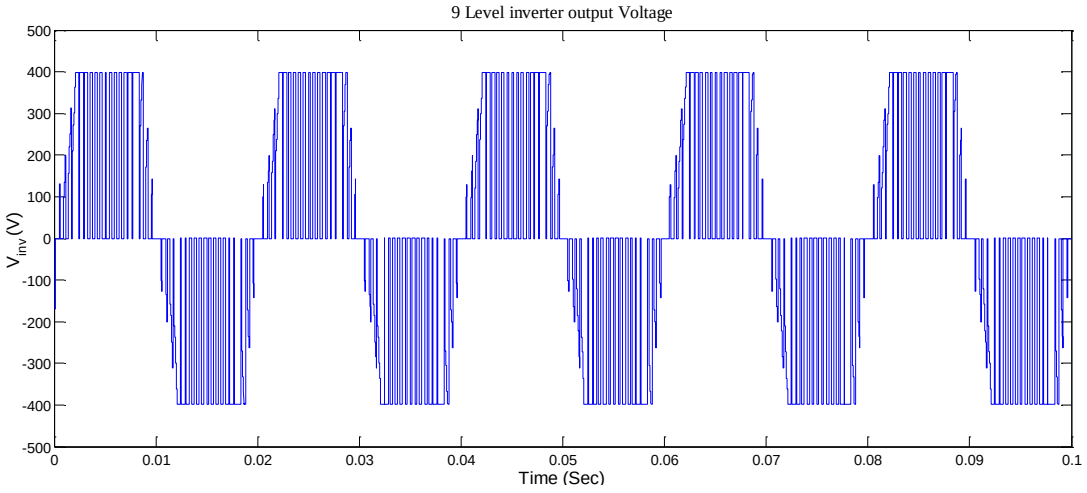
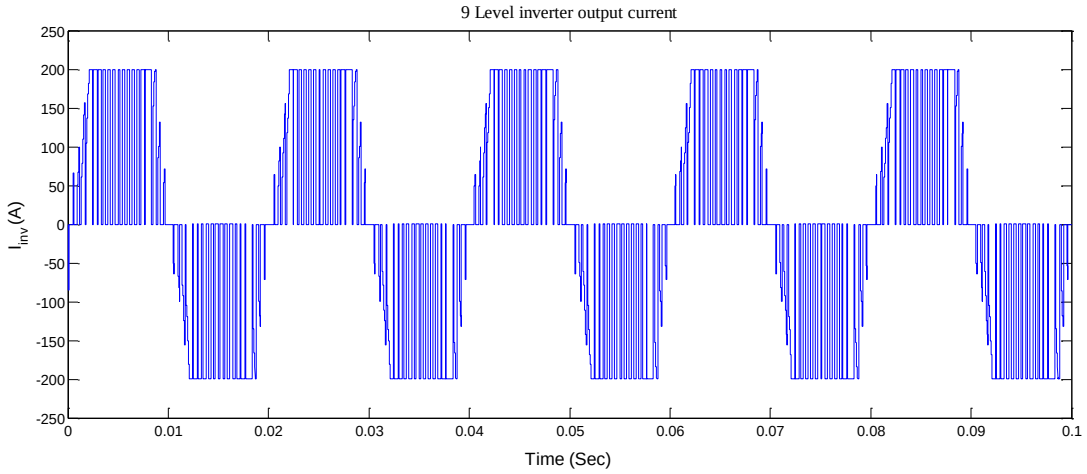


(a)



(b)

Figure 5 Proposed system (a) Voltage and (b) Current

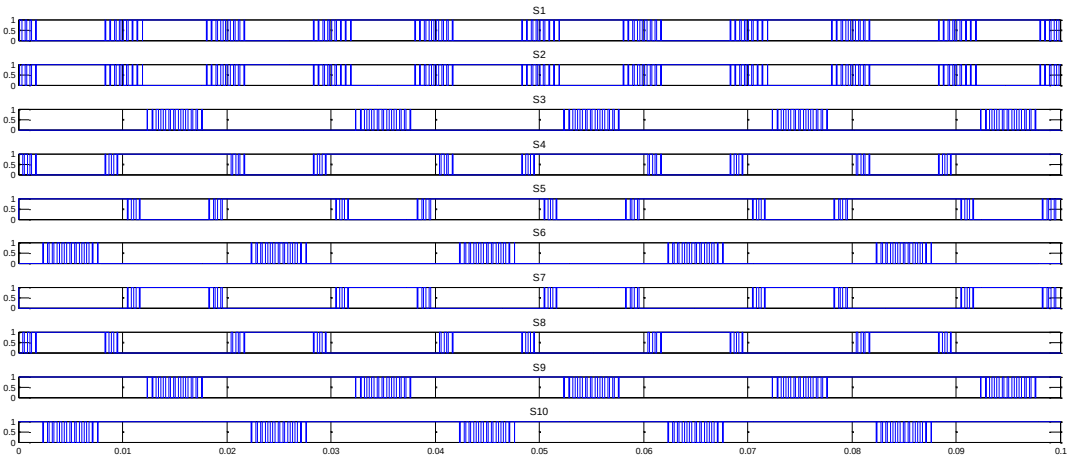


Figure 6 Switching pulse

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IV. Conclusion

A 9-level SCMLI of the boost type with a reduced number of components and two SCs was introduced in this study. Maintaining a steady-state voltage of Vin and 2Vin across SCs is achieved by charging them in parallel and discharging them in series. Thus, to simplify control, the proposed MLI does not have an auxiliary voltage balancing circuit. Additionally, MVS is limited to 2Vin, and there is a considerable reduction in voltage stress due to the synthesis of ac output that does not use a traditional full-bridge. No matter how long the circuit is, the MVS and the number of dc sources stay constant. Because of these unique characteristics, the suggested SCMLI works wonderfully in PV systems that only have one stage. The analysis of power loss, operational concepts, and the charging-discharging process have all been covered extensively. According to the results of the comparison, the suggested SCMLI manages to save costs significantly while keeping all the other benefits. The proposed 9-level SCMLI has been validated through both simulation.

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